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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/691,456	10/18/2000	Hisamitsu Suzuki	NECN 17.893	5653

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EXAMINER
GEBREMARIAM, SAMUEL A

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/691,456	SUZUKI, HISAMITSU	
	Examiner	Art Unit	
	Samuel A Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The limitation that the "annular diffused region having only one layer of material laid on top of said annular diffused region" is shown as just an intermediate product. In an operational final structure there will be more than one metallization layers formed over the annular diffused region. There is no final structure taught by applicant where there is only one material on top of the annular region. Therefore there is no support that shows a complete functional semiconductor device with only one layer on top of the annular diffused region.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1, in so far in compliance of 35 U.S.C. 112 and as best understood by the examiner is rejected under 35 U.S.C. 103(a) as being unpatentable over Hiramoto et al. US patent No. 5,661,329 in view of Seefeldt US patent No. 6,355,537.

Regarding claim 1, Hiramoto teaches (fig. 2) a semiconductor device comprising a silicon substrate 1, a bipolar transistor having a collector well (3) having a first conductivity type, an intrinsic base region (5) having a second conductivity type received in the collector well and an emitter region (6) having first conductivity type and received in the intrinsic base region, a first annular isolation trench (7) encircling the collector well, a second annular isolation trench (8) encircling the first annular isolation trench and an annular diffused region 2 (the area between annular isolation trenches 7 and 8), that is also in contact with first and second isolation trenches.

Hiramoto does not explicitly teach the annular diffused region (2) being second conductivity type.

It is conventional to dope the regions between isolation trenches with either p or n type conductivity.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the annular diffused region of Hiramoto's structure to have the conductivity type as claimed.

Hiramoto does not explicitly teach that the annular diffused region having only one layer of material laid on top of the annular diffused region.

It is conventional and also taught by Seefeldt (fig. 2) a diffused region (48) between two isolation trenches (26 and 24) having only one layer material (50) on top of the diffused region.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the single layer formed over the diffused region taught by Seefeldt in the structure of Hiramoto in order to form contact region.

Claims 2-10, in so far in compliance of 35 U.S.C. 112 and as best understood by the examiner is rejected are rejected as being unpatentable under 35 U.S.C. 103(a) as being unpatentable over Hiramoto and Seefeldt in view of Nii et al. US patent No. 5,933,719.

Regarding claim 2, Hiramoto teaches substantially the entire claimed structure, as applied to claim 1, above including, intrinsic base and collector well regions provided with both base and collector electrodes (column 5, lines 38-55).

Hiramoto does not teach base and collector electrodes and annular diffused regions are provided with a silicide layer on top thereof.

Nii teaches in fig. 20, a metal silicide formed on the base and collector electrode (column 13, lines 13-24).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a silicide layer in Hiramoto's device since silicides are known materials that are used for lowering contact resistance.

Regarding claim 3, Hiramoto teaches a semiconductor device as in claim 1 comprising a MOSFET (column 1, lines 11-20).

Regarding claim 4, Hiramoto teaches the annular diffused region includes annular sub-region including a plurality of first diffused regions and a second intermittent annular sub-region including a plurality of second diffused regions, and the first diffused regions and the second diffused regions are arranged alternately along the annular diffused region (fig 11c).

Regarding claim 5, Hiramoto teaches a third annular isolation trench between first intermittent annular region and second intermittent region (column 14, lines 38-68, column 15, lines 3-5).

Regarding claim 6, Hiramoto teaches a semiconductor device of claim 1,where the silicon substrate has a second conductivity type (column 5, lines 33-37).

Regarding claim 7, Hiramoto teaches a semiconductor device of claim 1, wherein the first conductivity type is n-type and the second conductivity-type is p-type.

Regarding claim 8, Hiramoto teaches (fig. 2) a semiconductor device as in claim 1, wherein the silicon substrate has a first conductivity-type, and includes a well having a second conductivity-type (2) and receiving therein the collector well (3).

Regarding claim 9, Hiramoto teaches the semiconductor device defined as in claim 8, wherein the bipolar transistor is a PNP transistor.

Regarding claim 10, Hiramoto teaches a semiconductor device as in claim 1, further comprising a third annular isolation trench (8) encircling second annular isolation trench, and another annular diffused region disposed between the second annular isolation trench and the third isolation trench while being in contact with the second and third isolation trenches (fig. 11c and column 14, lines 38-67, columns 15-16).

Response to Arguments

3. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is 703 305 1913. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Samuel Admassu Gebremariam
December 13, 2002

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800